44 GHZ MONOLITHIC LOW NOISE AMPLIFIER

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Abstract

The design, fabrication, and performance of a single-stage 44 GHz monolithic HEMT low noise amplifier are described. The chip includes a single heterojunction HEMT with matching and biasing circuits. Greater than 5 dB gain was measured from 43.5 to 45.5 GHz and a noise figure of 5 dB with the associated gain of 5.5 dB was achieved at 44.5 GHz. The chip size is 1.25mmx1.0mm.

Introduction

High Electron Mobility Transistors (HEMT) have demonstrated their superior electronic transport properties over the conventional MESFETs during the past few years. They are considered as a viable candidate device for a number of analog and digital applications. Notably among them are the microwave/millimeter-wave low noise amplifiers. State-of-the-art gain and noise performance have been demonstrated at high millimeter-wave frequencies from hybrid amplifiers using discrete HEMTs.[1,2] This paper presents the initial results of an effort to extend this hybrid technology to a monolithic one using a 44 GHz amplifier as a vehicle.

Design Considerations

The single stage monolithic amplifier design employed microstrip transmission line topology for easier implementation. The primary design factors considered here do not significantly change between the monolithic and hybrid approaches. The device structure selected for the monolithic design is largely determined by the availability of an accurate device model which is derived from thorough characterization of the discrete device in terms of its two-port and noise parameters at the operating frequencies. For the amplifier discussed here, a simpler structure as shown in Figure 1 was chosen because of the existence of an extensive S-parameter data base (up to 26 GHz) for this structure. Of course, this is not necessarily the optimal structure for lowest noise performance. In fact, there are other device features such as graded transition from the active layer to the top n+ contact layer and/or quantum well two-dimensional electron gas confinment that can readily improve the noise performance.

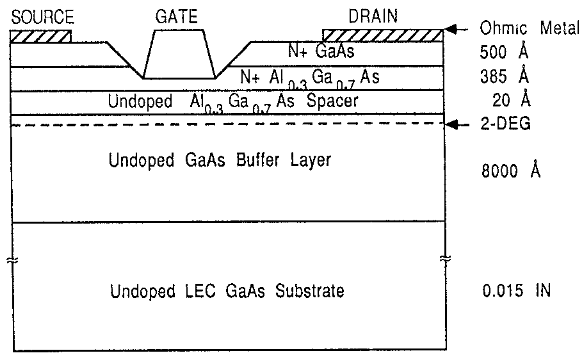

Figure 1. Cross-section of HEMT device

The model used (Figure 2) was derived from the S-parameter data measured on discrete HEMTs up to 26 GHz. In addition, this model was gain matched at several points around 40 GHz and S-parameter matched at 60 GHz to insure some millimeter-wave frequency responses. The HEMT geometry has a nominal gate length of 0.3μm, a total gate width of 80μm and 2μm source-drain separation and is in ground source configuration. The associated matching and biasing circuits were then optimized with the aid of a computer software.

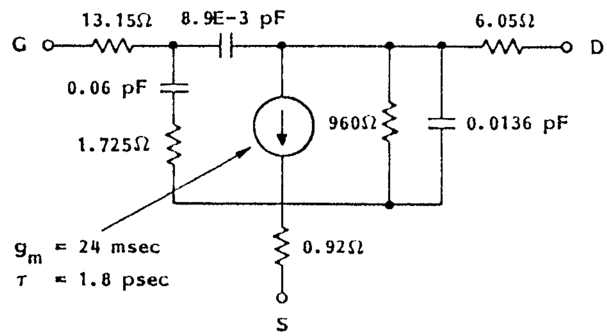

Figure 2. Intrinsic device model

Two types of single stage monolithic amplifiers were designed: one makes use of matching open stubs at both the input and output and the other used interdigitated capacitor input and open stub output matchings. Both designs are compatible with our HEMT process which is described later. The on-chip bias network was included in some circuits to achieve a higher level of integration and was designed to achieve out-of-band stability. Because of the inherent limitations from the underlying device structure, the final amplifier design was optimized for power gain at the expense of the noise performance.

Amplifier Fabrication

The HEMT device was fabricated on an aluminum gallium arsenide/gallium arsenide heterostructure which were grown by molecular beam epitaxy. The epi-material has 8,000 and 77,600 cm^2/V-sec Hall mobility for 10^{12} electrons/cm^2 at room and liquid nitrogen temperature respectively. The number of growth-related defects is less than 50 per cm^2 on a 0.8μm GaAs buffer.

TRW's baseline planar HEMT processing which is illustrated in Figure 3 was used to fabricate the single stage monolithic amplifier. Key features of this process include implant damage device isolation, extremely low resistance ohmic contacts, and self-aligned recessed gate using direct-write electron-beam lithography. Implant isolation permits surface planarity which is critical for uniform EBL gate resist processing. Ohmic contact resistivity of less than 0.08Ω-mm was obtained with alloyed Ni/AuGe/Ni/Au metallization.

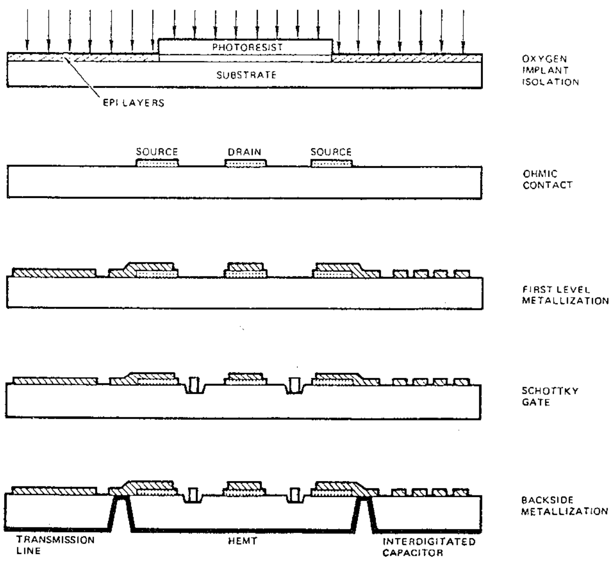

Figure 3. Monolithic HEMT IC process

The conventional gate geometry was defined with Cambridge EBMF-2 electron beam exposure system along with PMMA resist lift-off technique. 0.3μm gate length was routinely achieved. The substrate was subsequently thinned down to 0.1mm thick and via hole areas were defined by lithography. After chemical etching, the via and the rest of the backside were metallized with evaporated Ti/Au metallization. Individual chip was then separated by scribing. A sample circuit is shown in Figure 4.

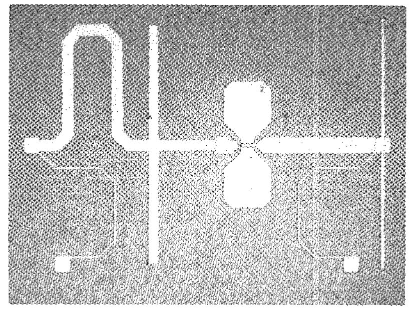

Figure 4. A sample monolithic amplifier circuit with open-stub matching and on-chip bias circuit

The DC characteristics of the HEMT device embedded in the monolithic amplifier circuits were measured and shown in Figure 5(a). The transconductance as a function of gate-source voltage is shown in Figure 5(b). Peak transconductance of 325 mS/mm was achieved.

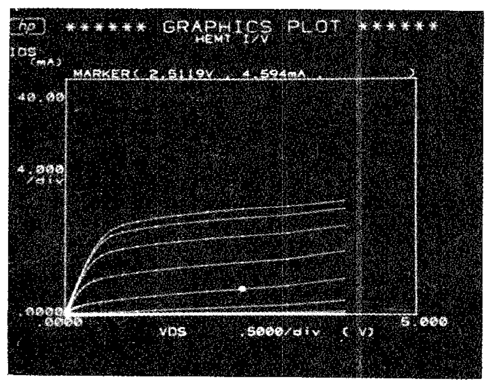

Figure 5(a) I-V characteristics of HEMT device

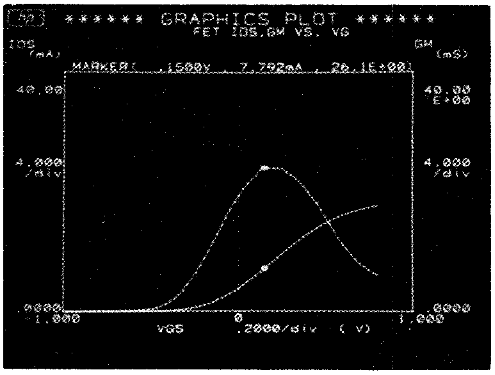

Figure 5(b) Transconductance and drain current versus gate-source voltage

Amplifier Characterization

The amplifier chip was epoxied onto a 5 mil ground plane pedestal which was inserted in a test fixture and charcterized with a waveguide measurement system via a pair of waveguide-finline-microstrip transitions. Two short gold wires were used to connect the transitions and theinput/output ports of the amplifier circuit. The finline transitions utilizes a chrome-gold metallization with the pattern photoetched onto a 10 mil thick highly polished quartz substrate. This type of transition has been extensively used at TRW and elsewhere and has shown good bandwidth, low insertion loss and low VSWR at millimeter-wave frequencies. Experimentally, insertion loss of 0.5 dB with return loss of better than 15 dB per transition was measured over more than 5 GHz bandwidth around 44 GHz.

The amplifier gain was measured with a scalar network analyzer from 42 to 47 GHz. The HEMT was biased at drain-source voltage of 4.0 volts and drain current of 10 mA for maximum gain. For those circuits without on-chip bias circuit, the bias was supplied through the finline transition via a quarter-wave high-low type bias network. The amplifier noise figure was spot measured with a Micronetics noise source and HP noise measurement system.

Results and Discussions

The predicted amplifier performance using the model described above is shown in Figure 6. Greater that 5 dB gain are expected over more than 2 GHz bandwidth around 44.5 GHz. In general, the measured gain response is also greater than 5 dB over the same frequency range but with a gain roll off at the lower end. Noise figure of 5 dB with an associated gain of 5.5 dB was measured at 44.5 GHz. For comparison, we had also constructed a single-stage hybrid amplifier using a discrete HEMT device from the same wafer slice as that of monolithic circuits. A minimum noise figure of 3.6 dB and 7.2 dB associated gain at 44.5 GHz were measured.

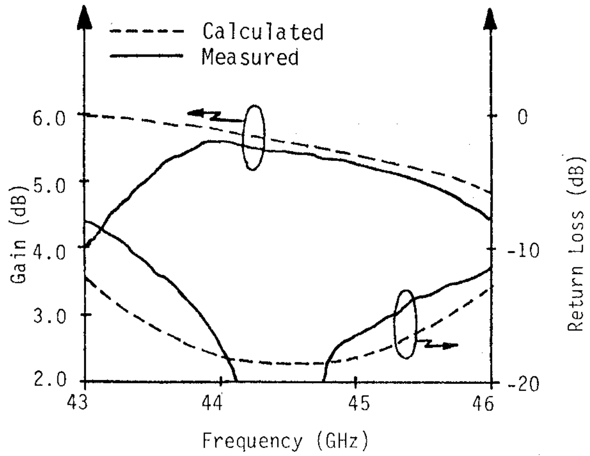

Figure 6. Calculated and measured amplifier gain and return loss

One of the goals for developing monolithic amplifiers is to achieve a first-pass success so that circuits can perform as designed without further tuning. However, this goal can only be attainable if the fabrication process is highly repeatable and accurate models for both the devices and the circuits are available to allow an accurate amplifier design at the desired operating frequencies. Therefore, the lower performance from the present monolithic amplifier is not unexpected. In fact, we believe that (1) present device model used even with gain or S-parameter matching at higher millimeter-wave frequencies may prove to be inadequate, (2) the device characteristics are known to deviate from the model due to the variations in the fabrication process; (3) since circuit features such as transmission line stubs, via holes, interdigitated capacitors, bonding wires, junctions and discontinuities were not adequately characterized at these frequencies at present, using their microwave frequency models in the design could lead to less than optimized performance (4) post-fabrication tuning which is available to hybrid amplifiers is almost impossible for monolithic amplifiers to overcome these problems. Nevertheless, we have demonstrated here that a reasonably good monolithic HEMT amplifier could still be fabricated at 44 GHz with a first order design and the existing fabrication process.

There are several ways to further improve the amplifier performance. For example, a more advanced device structure as previously mentioned could be employed to lower the intrinsic HEMT noise and thus lower the overall amplifier nois figure. The impact of process variations can b reduced with direct write electron beam lithography technique to define the matching and bias circuits on a wafer after the HEMT devices on the same wafer are adequately characterized. Such semi-customerized fabrication could be used to enhance the circuit yield at the expens of throughput. Of course, more accurate device and circuit models are always highly desirable to improve the overall amplifier performance. Currently, all these approaches are being pursued at TRW for the second generation monolithic amplifiers and we expect a higher performance monolithic HEMT amplifier should become available shortly.

Acknowledgement

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References

1. Michael Sholley, et al. "36.0 GHz Low Noise Amplifier" IEEE MTT Symposium, June 1985.
2. Michael Sholley, et al. "60 and 70 GHz Amplifiers" IEEE MTT Symposium, June 1986.